FAIRCHILD SEMICONDUCTOR®

December 2005

FDS6692A
N-Channel PowerTrench® MOSFET
30V, 9A, 11.5mΩ

Features

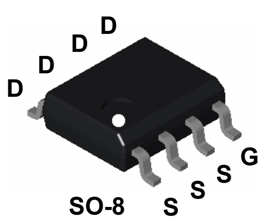
- $R_{DS(ON)}$ = 11.5mΩ, V_{GS} = 10V, I_D = 9A
- $R_{DS(ON)}$ = 14.5mΩ, V_{GS} = 4.5V, I_D = 8.2A
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low gate charge
- High power and current handling capability
- RoHS Compliant

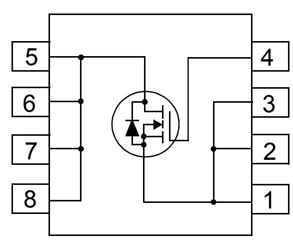
Applications

- DC/DC converters

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.





MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current		
	Continuous (T_A = 25°C, V_{GS} = 10V, $R_{\theta JA}$ = 85°C/W)	9	A
	Continuous (T_A = 25°C, V_{GS} = 4.5V, $R_{\theta JA}$ = 85°C/W)	8.2	A
	Pulsed	48	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	240	mJ
P_D	Power dissipation	1.47	W
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient at 10 seconds (Note 3)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient at 1000 seconds (Note 3)	85	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS6692A	FDS6692A	SO-8	330mm	12mm	2500 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	30	-	-	V
$\frac{\Delta B_{VDSS}}{\Delta T_J}$	Breakdown Voltage Temp. Coefficient	I_D = 250μA, Referenced to 25°C	-	21	-	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V	-	-	1	μA
		V_{GS} = 0V, T_J = 150°C	-	-	250	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	1.2	-	2.5	V
$\frac{\Delta V_{GS(TH)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	-	-5	-	mV/°C
$R_{DS(ON)}$	Drain to Source On Resistance	I_D = 9A, V_{GS} = 10V	-	8.2	11.5	mΩ
		I_D = 8.2A, V_{GS} = 4.5V	-	11	14.5	mΩ
		I_D = 9A, V_{GS} = 10V, T_J = 150°C	-	13	19	mΩ
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz	-	1210	1610	pF
C_{OSS}	Output Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz	-	330	440	pF
C_{RSS}	Reverse Transfer Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz	-	138	210	pF
R_G	Gate Resistance	f = 1MHz	-	2.0	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V; V_{DD} = 15V, I_D = 9A, I_g = 1.0mA	-	22	29	nC
$Q_{g(5)}$	Total Gate Charge at 5V	V_{GS} = 0V to 5V; V_{DD} = 15V, I_D = 9A, I_g = 1.0mA	-	12	16	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0V to 1V; V_{DD} = 15V, I_D = 9A, I_g = 1.0mA	-	0.93	1.2	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 15V, I_D = 9A, I_g = 1.0mA	-	3	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau	V_{DD} = 15V, I_D = 9A, I_g = 1.0mA	-	2.1	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	V_{DD} = 15V, I_D = 9A, I_g = 1.0mA	-	4.8	-	nC

Switching Characteristics (V_{GS} = 10V)

t_{ON}	Turn-On Time	V_{DD} = 15V, I_D = 9A V_{GS} = 10V, R_{GS} = 6.2Ω	-	-	60	ns
$t_{d(ON)}$	Turn-On Delay Time		-	8	-	ns
t_r	Rise Time		-	32	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	33	-	ns
t_f	Fall Time		-	13	-	ns
t_{OFF}	Turn-Off Time		-	-	69	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	I_{SD} = 9A	-	-	1.25	V
		I_{SD} = 2.1A	-	-	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 9A, dI_{SD}/dt=100A/µs	-	-	27	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 9A, dI_{SD}/dt=100A/µs	-	-	17	nC

Notes:

1: Starting T_J = 25°C, L = 9.2mH, I_{AS} = 7.2A, V_{DD} = 30V, V_{GS} = 10V.

2: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

3: $R_{\theta JA}$ is measured with 1.0 in^2 copper on FR-4 board

Typical Characteristics T_J = 25°C unless otherwise noted

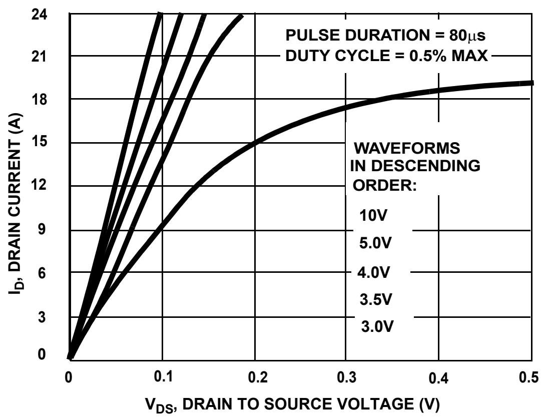


Figure 1. On Region Characteristics

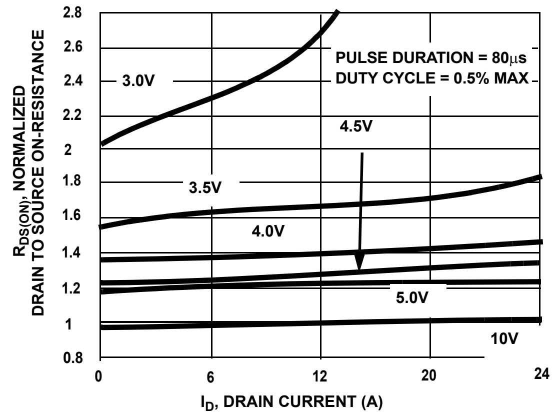


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

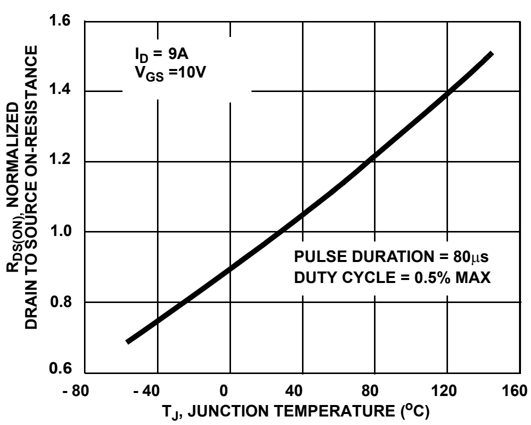


Figure 3. On Resistance Variation with Temperature

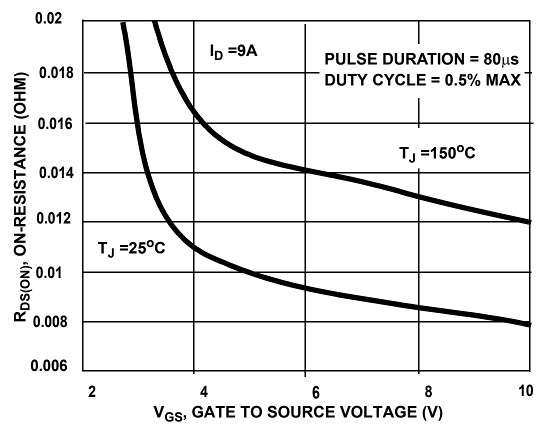


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

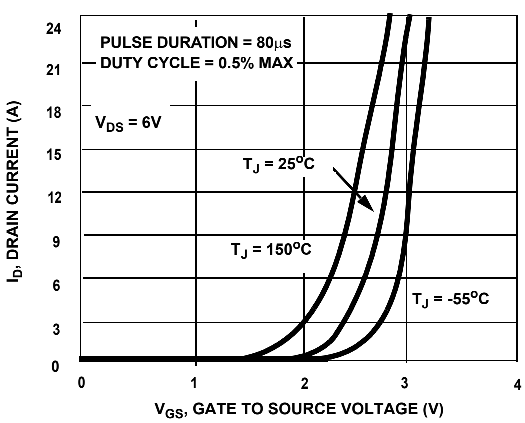


Figure 5. Transfer Characteristics

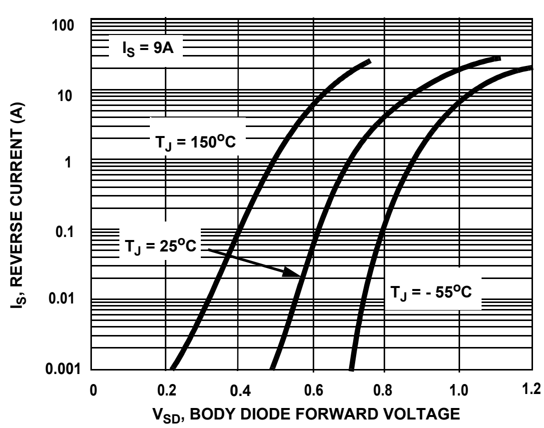


Figure 6. Body Diode Forward Voltage Variation With Source Current and Temperature

Typical Characteristics T_J = 25°C unless otherwise noted

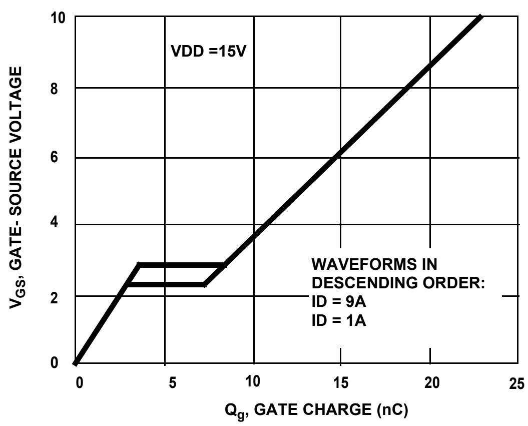


Figure 7. Gate Charge Characteristics

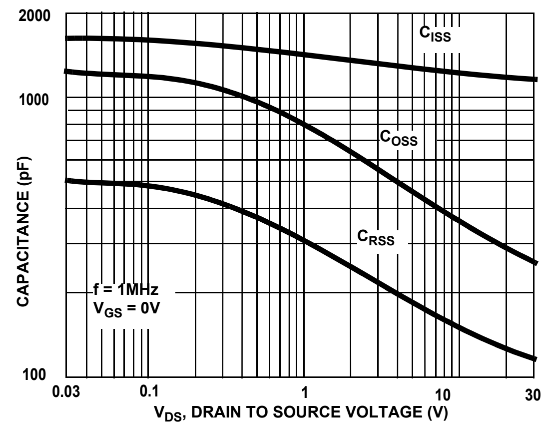


Figure 8. Capacitance Characteristics

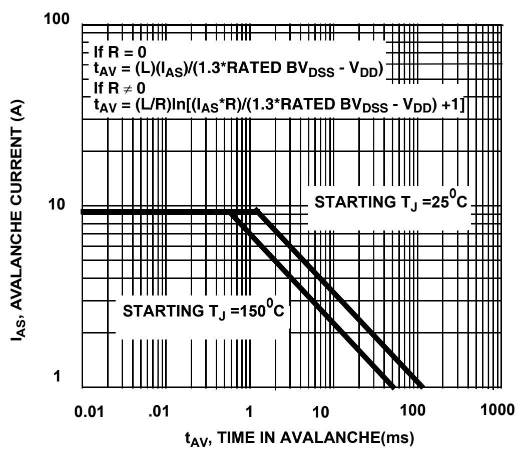


Figure 9. Unclamped Inductive Switching Capability

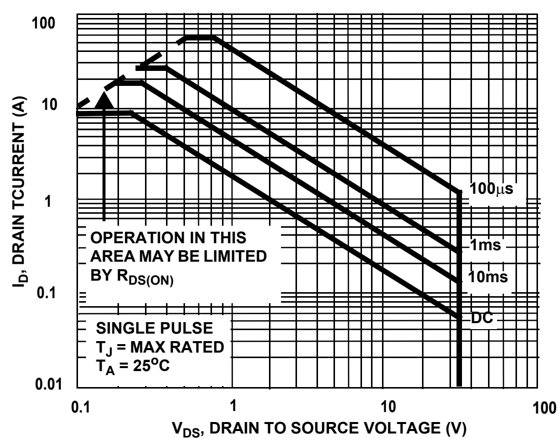


Figure 10. Safe Operating Area

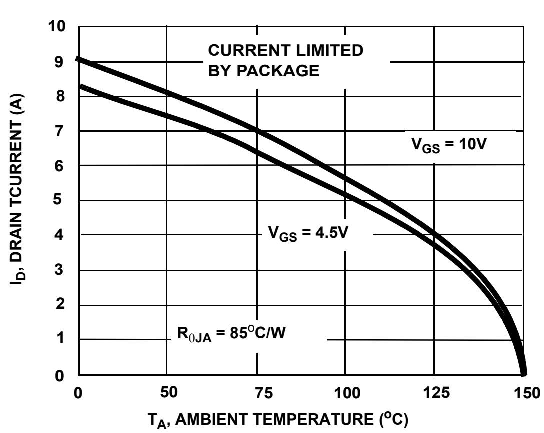


Figure 11. Maximum Continuous Drain Current vs Ambient Temperature

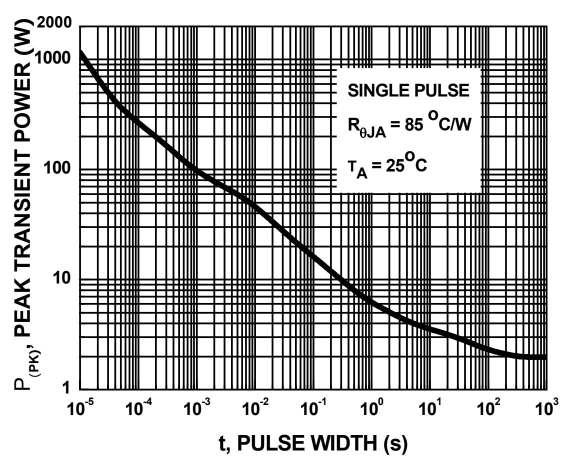


Figure 12. Single Maximum Power Dissipation

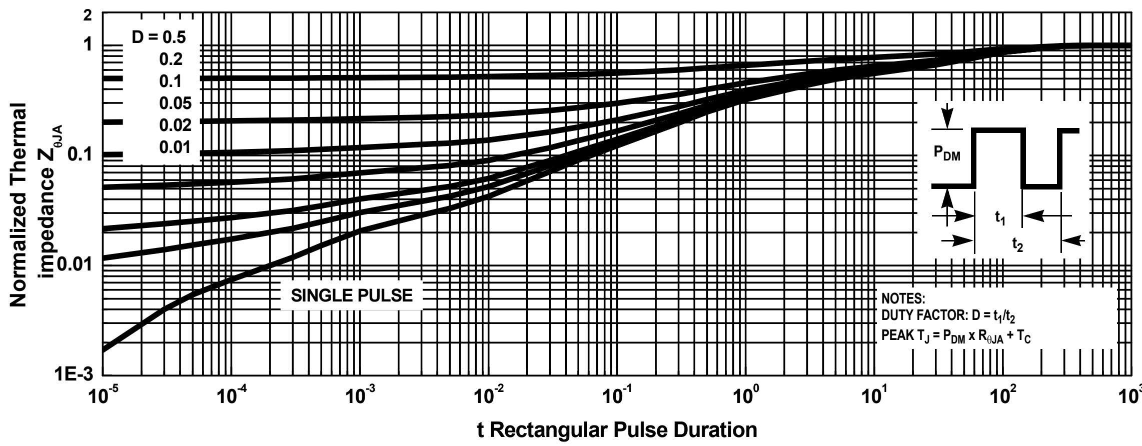


Figure 13. Transient Thermal Response Curve

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